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TABITHA JOHNSON
(SENDER'S PRINTED NAME)

(SIGNATURE)

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Enclosed for filing is a patent application under 37 CFR 1.53(b) of:
Inventor: **Tae-Gyoung KANG**
For: **LAYOUT METHOD OF SEMICONDUCTOR DEVICE**

Enclosures:
[X] Specification (pages 1-14); claims (pages 15-20); abstract (page 21)
[X] 17 sheet(s) of formal drawings
[X] Executed Combined Declaration and Power of Attorney
[X] Executed Assignment
[X] Korean Priority Document #98-63134, filed December 31, 1998
[X] Any deficiency or overpayment should be charged or credited to deposit account number 13-1703

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Respectfully submitted,

MARGER JOHNSON & McCOLLOM P.C.

Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM P.C.
1030 S.W. Morrison Street Portland OR 97205 (503) 222-3613

LAYOUT METHOD OF SEMICONDUCTOR DEVICE

Field of the Invention

The present invention relates to a layout method of a semiconductor device, and more particularly to the layout method of the semiconductor device to reduce the variance in process deviations which may occur during photo and etching processes.

Background of the Invention

As progress is made in functions of a system to which a semiconductor device is applied, functions of high speed and high integration in the semiconductor device have become important to the semiconductor device. Accordingly, the layout method is as important as the circuit design and fabricating in response to the trend of high speed and high integration of the semiconductor device.

Some fabricating techniques for conventional semiconductor device, e.g., the uneven light reflection of the photo process and non-uniformity of the etching process, have brought about variances in process deviations at gates of transistors.

The process deviation depends upon the extent of differences in the length of the gates when measured before and after the photo process. Some process deviation is to be expected and is quite acceptable when it is uniform as among various gates. When it is not substantially uniform, i.e., if there is a great variance in the process deviation, the threshold voltage of the transistors fluctuates, thereby leading to malfunctions of the semiconductor device. In other words, the device may operate differently from what the designer intends it to.

Thus, great efforts have been made to minimize the variances in the process deviations which may occur in the course of manufacturing the semiconductor device.

Fig. 1 is a schematic diagram for explaining problems in the photo masking process, one of the manufacturing processes of a semiconductor device, comprising silicon 10, silicon dioxide 12, aluminum 14, photo resist 16, transparent glass 18, and opaque layer 20.

When the photo process is performed with the photo resist 16 being covered over the aluminum 14, the aluminum 14 does not absorb light, instead, the aluminum reflects light as shown in Fig. 1. Moreover, aluminum 14 is disposed in certain areas with a slant angle of θ, and thus reflects light obliquely on the slant surface, so that a photo pattern is not formed precisely as desired.

However, the layout method of the conventional semiconductor device is to arrange gates without a regular gap between gates. The result is that the slant angle of θ as between gates is not kept constant. As a result, the angle of reflecting light becomes different between gates, despite nearly identical photo masking and etching processes, to bring about a potentially wide variance in process deviations at the gates.

Fig. 2 is a schematic diagram for explaining a problem in the etching process, one of the manufacturing processes of the semiconductor device, comprising silicon 10, silicon dioxide 12 and photo resist 16.

As shown in Fig. 2, etching of the oxide layer through open regions of photo resist 16 produces undercut of silicon dioxide 12, as described by circles that increase in radius to the depth of silicon 10. The greater the radius of the circle, the more deeply the photo resist 16 gets undercut. The extent to which the photo resist 16 may be undercut cannot be known until the photo resist 16 is removed. But the shape of the edge of the oxide layer pattern (as shown with dot lines in Fig. 2) is a good indicator of the degree of undercut. In other words, the etching process is not uniform thereby producing undesirable process deviations. These etching process deviation also vary widely between gates having irregular gaps therebetween.

Therefore, there is a problem in the layout method of the conventional semiconductor device, in that the gates of transistors conventionally are arranged with irregular gaps. As a

result, the gates reflect light differently in the photo process and do not uniformly etch the layer in the etching process, thereby increasing process variances.

In addition, as the layout method of neighboring circuits of the conventional semiconductor device is the same as that of the aforementioned general semiconductor device, the extent of process deviations gets bigger during photo and etching processes.

Especially, a sense amplifier of the semiconductor device is a circuit for amplifying and outputting a very small voltage difference of input signals, so that it is very sensitive. Therefore, it is important to correct differences of threshold voltages of transistors which make up the sense amplifier. However, as the layout method of the conventional sense amplifier is the same as that of the general semiconductor device, variances in the process deviations during the photo and etching processes increases.

In other words, the variance in process deviations of the etching process is added to that of the photo process, thereby increasing overall variances in the fabrication process.

As described above, the problems in those photo and etching processes have already been well known, so that it is necessary to minimize the variances in process deviations because the variances in process deviations caused at the gates during those processes may bring about changes in the threshold voltage of transistors.

Summary of the Invention

It is an object to provide a layout method of a semiconductor device to minimize the variances in process deviations which may occur in photo and etching processes.

It is another object to provide a layout method of neighboring circuits of the semiconductor memory device to minimize the variances in process deviations which may occur in photo and etching processes.

It is also another object to provide a layout method of a sense amplifier of the semiconductor device to minimize the variances in process deviation which may occur in photo and etching processes.

In order to accomplish the aforementioned first object, there is provided a layout method of a semiconductor device comprising the steps of:

arranging active regions of a plurality of transistors having at least more than one first and second electrodes disposed on a substrate;

arranging a plurality of gates of transistors between more than one first and second electrodes of those active regions respectively by positioning at least more than one gates having predetermined width and length at a constant gap on the substrate; and

arranging a plurality of dummy gates having predetermined width and length between a plurality of transistors or between and outside transistors at the same gap as that of the gates of transistors on the substrate.

In order to accomplish the aforementioned second object, there is provided a layout method for a neighboring circuit of the semiconductor device, the same method as that of the aforementioned semiconductor device.

In order to accomplish the aforementioned third object, there is provided a layout method for a sense amplifier of a semiconductor device having input transistors for data and control signals in accordance with the aforementioned layout method of a semiconductor device.

Brief Description of the Drawings

Fig. 1 is a schematic diagram for explaining a problem in a photo process.

Fig. 2 is a schematic diagram for explaining a problem in an etching process.

Fig. 3 is a block diagram illustrating the layout of an embodiment of a conventional semiconductor memory device.

Fig. 4 is a circuit diagram of a conventional sense amplifier.

Figs. 5 through 10 are diagrams illustrating the layout of the sense amplifier of Fig. 4 in accordance with a conventional layout method.

Fig. 11 is a diagram illustrating the layout of the sense amplifier of Fig. 4 in accordance with a first invented layout method.

Fig. 12 through 17 are diagrams illustrating the layout of the sense amplifier shown in Fig. 4 in accordance with a second invented layout method.

Fig. 18 is a graph illustrating variances in process deviations in accordance with the conventional layout method and the layout method of the present invention.

Detailed Description of the Invention

Fig. 3 is a block diagram illustrating the layout of an embodiment of a conventional semiconductor memory device, comprising memory cell array blocks 30-1, 30-2, ... 30-n, block row decoders 32-1, 32-2, ...32-n, a bit line pre charge circuit 34, a block selector 36, a column selection gate 38, a sense amplifier/ light driver 40, a column decoder 42, a wide zone row decoder 44, a column address input buffer 46, a data input/output buffer 48, a control signal input buffer 50 and a row address input buffer 52.

The layout of the prior art semiconductor memory device includes the memory cell array 30 and neighboring circuits of controlling data input/output to the memory cell array 30.

However, there is a problem in the conventional layout method of neighboring circuits of the semiconductor device in that the transistor gates of the neighboring circuits have been arranged at an irregular gap in the conventional layout method of the semiconductor device, thereby increasing a variances in process deviations at the transistor gates in the course of the photo and etching processes.

In addition, there is another problem in the conventional layout method of the semiconductor device in that the increase in variances in process deviations as such has caused the semiconductor device not to operate properly as the designer intends it to.

Now, the conventional layout method of the semiconductor memory device and that of the present invention will be compared and explained by using the sense amplifier among the neighboring circuits.

Fig. 4 is a circuit diagram for illustrating the structure of the conventional sense amplifier, comprising PMOS transistors P1, P2, P3 and NMOS transistors N1, N2, N3, N4. Also shown in Fig. 4 are control signal line CON input signal D, input signal DB and output signal OUT.

Figs. 5 through 10 illustrate the layout of the sense amplifiers shown in Fig. 4 in accordance with the conventional layout method.

Fig. 5 illustrates the layout of sources, drains and gates of the transistors which make up the sense amplifier.

In Fig. 5, the sources, drains and gates of the PMOS transistors P1, P2, P3 are respectively denoted with P1S, P2S, P3S, P1D, P2D, P3D, and P1G, P2G, P3G, while the sources, drains and gates of the NMOS transistors N1, N2, N3, N4 are respectively denoted with N1S, N2S, N3S, N4S, N1D, N2D, N3D, N4D and N1G, N2G, N3G, N4G. Reference numerals 60, 66 are bias lines while reference numerals 62, 64 are power lines. In addition, symbols W1, W2 and L are respectively width and length of the transistors.

First of all, the gates of the PMOS transistors P1, P2, P3 and those of the NMOS transistors N1, N2, N3, N4 are divided from one common terminal into two and, then, separately arranged. The width W1 of the gates of the NMOS transistors N1, N2 is smaller than that W2 of the gates of the PMOS transistors P1, P2, P3 and those of the NMOS transistors N3, N4. On the other hand, the length L of the gates of the PMOS transistors P1, P2, P3 is the same as that of the NMOS transistors N1, N2, N3, N4.

According to the conventional layout method shown in Fig. 5, gaps (a) between separate gates of all transistors are constant, while gaps (b, c, d) between the other gates of those transistors are inconstant. Therefore, uneven light reflection in the photo process and non-uniformity of the etching process result in increase in the variances in process deviations.

Fig. 6 illustrates contacts formed in the layout shown in Fig. 5, that is, the contacts being formed on the sources, drains, a gate common terminal, power lines, and bias lines of the PMOS transistors P1, P2, P3 and NMOS transistors N1, N2, N3, N4. In Fig. 6 the portions 70 marked with squares indicate where the contacts are formed.

Fig. 7 illustrates metals ME1 formed at the contacts shown in Fig. 6, that is, the metals being formed all over the contacts 70 and power lines 60, 66 (not visible in Fig. 7). In Fig. 7, the portions marked with horizontally slanting lines indicate where the metals are formed.

Fig. 8 illustrates contacts formed at the metals shown in Fig. 7, and the portions 72 marked with dark squares indicate where the contacts are formed.

Fig. 9 illustrates metal lines formed along with the contacts shown in Fig. 8, and the portions ME2 marked with vertically slanting lines are where the metals are formed. Thus, the gates, drains, sources of the transistors of the sense amplifier shown in Fig. 4 are connected by metals. In Fig. 9, the metal lines 74, 76, 78, 80 respectively indicate control signal CON applying line, input signal D applying line, other input signal DB applying line and gate connecting line of the PMOS transistor P1 and NMOS transistors N1, N2.

Fig. 10 illustrates metals ME3 for applying power voltage and grounding voltage to the metal lines ME2. The striped portions, marked with dots, indicate where the metals ME3 are formed, while the portions 82 marked with lattices indicate where VIA contacts are formed. The portions 82 and metals ME3 are connected to apply the power voltage and grounding voltage.

Fig. 5 has shown the problem in the conventional layout method of the semiconductor memory device. The diagrams shown in Figs. 6 through 10 have briefly illustrated the layout of the sense amplifier shown in Fig. 4. The inconstancy, or non-uniformity, of gaps on the semiconductor are described and illustrated in Fig. 5 at a, b, and d, and are clear from the non-uniformity of feature column spacing in Figs. 6-10.

On the other hand, Fig. 11 illustrates a layout of a semiconductor memory device in accordance with an embodiment of the present invention. Dummy gates DG1, DG2 having the same gap (a) as gates divided in the layout shown in Fig. 5 are additionally assembled at the space among gates of the transistors which make up the sense amplifier.

A common line connecting the dummy gates DG1, DG2 is shown in Fig. 11, but it can be properly divided and installed.

The dummy gates thus constructed do not exert any influence upon operations of the circuits of the sense amplifier, but advantageously exert a beneficial influence on the semiconductor fabrication processes.

After all the gates are completely disposed as previously described in Fig. 11, the rest of the layout of the semiconductor device can be arranged according to the conventional or any other layout method.

In other words, according to the layout method of the sense amplifiers of the present invention shown in Fig. 11, there are the gates which perform actual operations of the sense amplifier while the dummy gates are positioned between or outside those actually operating gates without making any influence on the actual operations of the sense amplifier.

However, the installation of the dummy gates minimizes the variances in the process deviations which may occur in the photo and etching processes for the production of the semiconductor device.

Figs. 12 through 17 illustrate a layout method of the sense amplifier shown in Fig. 4 in accordance with another embodiment of the present invention.

In Fig. 12, the sources, drains and gates of the PMOS transistors P1, P2, P3 are respectively denoted with P1S, P2S, P3S, P1D, P2D, P3D, and P1G, P2G, P3G, while the sources, drains and gates of the NMOS transistors N1, N2, N3, N4 are respectively denoted with N1S, N2S, N3S, N4S, N1D, N2D, N3D, N4D and N1G, N2G, N3G, N4G. Reference numerals 60, 66 are bias lines while reference numerals 62, 64 are power lines. In addition,

symbols DG1, DG2, DG3, DG4, DG5, DG6 respectively indicate dummy gates formed at the same gap (a) as that of the gates divided between and outside the transistors.

First of all, gates of the PMOS transistors P1, P2, P3 and those of the NMOS transistors N3, N4 are divided from one common terminal into four and separately arranged. As a result, the sources and drains of the transistors are respectively divided into three and two for the arrangement.

Symbol L indicates the length of the gates of the transistors P1, P2, P3, N1, N2, N3, N4 and that of the dummy gates DG1, DG2, DG3, DG4, DG5, DG6. On the other hand, symbols W2/2, W1/2, W3, W5, and W4 respectively indicate the width of the gates of the PMOS transistors P1, P2, P3 and the NMOS transistors N3, N4, that of the gates of the NMOS transistors N1, N2, that of the dummy gates DG5, DG6, that of the dummy gates DG1, DG4, and that of the dummy gates DG2, DG3. Dummy gate widths W3 and W4 may be seen to vary, as shown, depending upon the placement and gate widths of PMOS transistors P1, P2, P3 and NMOS transistors N1, N2, N3, N4.

As shown in Fig. 12, the gap (a) between the divided gates which compose a single transistor is the same as that between the various transistors.

There is a difference between the layouts shown in Figs. 5 and 12 in additional arrangement of dummy gates DG1, DG2, DG3, DG4, DG5, DG6.

Although one gate has been divided into four as in the aforementioned embodiment, it will be understood by those skilled in the art that a gate may be divided into more than four.

In the present invention, the gates are arranged at a constant gap (a) as shown in Fig. 12 to thereby reduce the variances in process deviations.

Fig. 13 illustrates contacts formed in the layout shown in Fig. 12, that is, the contacts being formed on the sources, drains, gate common terminals and bias lines of the PMOS transistors P1, P2, P3 and NMOS transistors N1, N2, N3, N4. In Fig. 13 the portions 90 marked with squares indicate where the contacts are formed.

Fig. 14 illustrates metals ME1 formed at the contacts shown in Fig. 13, that is, the metals being formed all over the contacts 90 and power lines 60, 66. In Fig. 14, the portions ME1 marked with horizontally slanting lines indicate where the metals are formed.

Fig. 15 illustrates contacts formed at the metals ME1 shown in Fig. 14, and the portions 92 marked with dark squares indicate where the contacts are formed.

Fig. 16 illustrates metal lines formed along with the contacts shown in Fig. 15, and the portions ME2 marked with vertically slanting lines are where the metals are formed. Thus, the transistors of the sense amplifier shown in Fig. 4 are connected with metals. The metal lines 94, 96, 98, 100 respectively indicate a control signal CON applying line, a data D input line, another data DB input line and an output signal OUT generating line.

A power voltage applying line 102 and a grounding voltage applying line 104 are illustrated in Fig. 17.

Fig. 12 illustrates the layout method of the sense amplifiers in accordance with another embodiment of the present invention. However, the layout shown in Figs. 13 through 17 may be in a different arrangement. The drawings shown in Figs. 13 through 17 here are to show an actual example of the sense amplifier in accordance with the present invention.

It is a unique characteristic of the present invention that the dummy gates having no influence upon actual operations of transistors are arranged between and outside the gates formed for actual operations of transistors. In accordance with the invention, all of those divided gates are arranged at a constant gap, thereby minimizing the variances in process deviations that may occur in the photo and etching processes.

In the aforementioned embodiment, the dummy gates are arranged between and outside the gates of transistors. However, it may be also possible for the dummy gates to be arranged only between the gates of transistors.

Fig. 18 is a graph for illustrating variances of the process deviations in case layouts of the semiconductor device are made in accordance with the conventional method or that of the

present invention. The horizontal axis shows the number of measured gates while the vertical axis shows the process deviations (that is, the length μm of the gates respectively measured).

After the gates of transistors of the semiconductor device are manufactured in accordance with a conventional layout method or that of the present invention, the process deviations of those seventeen gates are measured. As a result, it has been found that the gates of the transistors arranged in the layout method of the present invention shows a smaller variances in process deviations than that of the conventional layout method. The maximum, minimum and average values of process deviations and its variance are shown in the following Table.

unit (μm)	conventional method	method of the present invention
maximum process deviation	0.234μm	0.221μm
minimum process deviation	0.226μm	0.218μm
average process deviation	0.233μm	0.223μm
variance in deviation (μm)	0.008μm	0.003μm

As shown in Table, the variances in process deviations has been decreased by as much as 0.005μm when the layout method of the present invention is applied instead of the conventional layout method.

As shown in the aforementioned embodiment of the present invention, the layout method of the sense amplifier of the semiconductor device has been explained. Also, the layout method of the present invention may be applied to the semiconductor device or the neighboring circuits of the semiconductor memory device, thereby minimizing the variances in process deviations.

Furthermore, the transistors to which the data signals of the sense amplifier are input and the transistors to which the enable signals of the sense amplifier are input, that is, the PMOS transistors P1, P2, P3 and the NMOS transistors N1, N2, N3, N4 of the circuit shown in Fig. 4, are arranged in accordance with the layout method of the present invention, thereby reducing the variances in process deviations and difference of the threshold voltage.

According to the layout method of the present invention, all the gates of the transistors which compose of circuits of the semiconductor device or other neighboring circuits of the semiconductor memory device are arranged at a constant gap by additionally installing dummy gates.

The dummy gates are arranged to keep all those gates at a constant gap between and outside (or only between) the gates which have been already formed for actual operations, thereby minimizing the variances in process deviations which may occur in the photo and etching processes.

Therefore, there is an advantage in the layout method of the present invention in that the dummy gates are additionally installed to arrange the gates of the transistors composing of the neighboring circuits at a constant gap, thereby minimizing the variances in process deviations.

In addition, there is another advantage in the layout method of the present invention in that the variances in process deviations is minimized to reduce the difference in the threshold voltage, thereby improving reliability of the semiconductor memory device.

Having illustrated and described the principles of my invention in a preferred embodiment thereof, it should be readily apparent to those skilled in the art that the invention can be modified in arrangement and detail without departing from such principles. I claim all modifications coming within the spirit and scope of the accompanying claims.

What is claimed is:

1. A layout method of a semiconductor device comprising the steps of:

arranging active regions of a plurality of transistors, the active regions having at least more than one first and second electrodes disposed on a substrate;

arranging a plurality of gates of transistors between the more than one first and second electrodes of those active regions by positioning at least two or more gates having predetermined width and length at a substantially constant gap on the substrate; and

arranging a plurality of dummy gates having predetermined width and length between a plurality of transistors at substantially the same gap as that of the gates of transistors on the substrate.

2. The method, as defined in claim 1, wherein the length of the dummy gates is the same as that of the gates of the transistors.

3. The method, as defined in claim 1, wherein at least more than one gate of the plurality of transistors have common terminals each of which is commonly connected on the substrate of the semiconductor device.

4. The method, as defined in claim 1, wherein a plurality of dummy gates are commonly connected on the substrate.

5. A layout method of sense amplifier of a semiconductor device, wherein the sense amplifier amplifies and outputs the difference between the first and second input data applied by data input transistors and more than one control signal input transistors to which the control signals are applied, the method comprising the steps of:

arranging active regions of a plurality of transistors, the active regions having at least more than one first and second electrodes disposed on a substrate;

arranging a plurality of gates of transistors between more than one first and second electrodes of those active regions respectively by positioning two or more gates having predetermined width and length at a substantially constant gap on the substrate; and

arranging a plurality of dummy gates having predetermined width and length between the data and control signal input transistors at substantially the same gap as that of the gates divided from the data and control signal input transistors on the substrate.

6. The method, as defined in claim 5, wherein the dummy gates have a predetermined width, that is, the same as that of the gates which are largest in width among those divided gates of a plurality of transistors.

7. The method, as defined in claim 5, wherein the length of the dummy gates is substantially the same as that of the gates.

8. The method, as defined in claim 5, wherein at least more than one gate of the data and control signal input transistors have common terminals each of which is commonly connected on the substrate.

9. The method, as defined in claim 5, wherein a plurality of dummy gates are commonly connected on the substrate.

10. A layout method of a semiconductor device comprising the steps of:

arranging active regions of a plurality of transistors having at least more than one first and second electrodes disposed on a substrate;

arranging a plurality of gates of transistors between more than one first and second electrodes of those active regions respectively by positioning at least more than one gates having predetermined width and length at a substantially constant gap on the substrate; and

arranging a plurality of dummy gates having predetermined width and length between and outside a plurality of transistors at substantially the same gap as that of the gates of transistors on the substrate.

11. The method, as defined in claim 10, wherein the length of the gates of the transistors is substantially the same as that of the dummy gates.

12. The method, as defined in claim 10, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate of the semiconductor device.

13. The method, as defined in claim 10, wherein a plurality of dummy gates are commonly connected on the substrate.

14. A semiconductor device comprising:

a substrate;

active regions of a plurality of transistors, the active regions having at least more than one first and second electrodes on the substrate;

a plurality of gates of transistors disposed on the substrate between more than one first and second electrodes of those active regions respectively, wherein two or more gates are of a predetermined width and length at a substantially constant gap on the substrate; and

a plurality of dummy gates having predetermined width and length between a plurality of transistors at substantially the same gap as that of the gates of transistors on the substrate.

15. The device, as defined in claim 14, wherein the length of the dummy gates is substantially the same as that of the gates of the transistors.

16. The device, as defined in claim 14, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

17. The device, as defined in claim 14, wherein a plurality of dummy gates are commonly connected on the substrate.

18. A semiconductor device comprising:

a substrate;

active regions of a plurality of transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of gates of transistors disposed between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate is of predetermined width and length at a substantially constant gap on the substrate; and

a plurality of dummy gates having predetermined width and length between and outside a plurality of transistors at substantially the same gap as that of the gates of transistors on the substrate.

19. The device, as defined in claim 18, wherein the length of the dummy gates is substantially the same as that of the gates of the transistors.

20. The device, as defined in claim 18 wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

21. The device, as defined in claim 18, wherein a plurality of dummy gates are commonly connected on the substrate.

22. A semiconductor device comprising:

a substrate;

active regions of a plurality of transistors having at least more than one first and second electrodes disposed on the substrate;

a plurality of gates of transistors between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate has a predetermined width and length at a substantially constant gap on the substrate; and

a plurality of dummy gates having predetermined width and length outside a plurality of transistors at substantially the same gap as that of the transistor gates on the substrate.

23. The device, as defined in claim 22, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

24. The device, as defined in claim 22, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

25. The device, as defined in claim 22, wherein a plurality of dummy gates are commonly connected on the substrate.

26. A semiconductor device comprising:

a substrate;

active regions of transistor, the active regions having at least one first and second electrodes on the substrate;

at least one gate layer disposed on the active regions between the first and second electrode, wherein the gate electrode layer is a predetermined width and length; and

a plurality of dummy gate layers disposed between and outside of the active region and having predetermined width and length at a substantially constant gap from the gate layer.

27. The device, as defined in claim 26, wherein the lengths of the dummy gates layers are substantially the same as that of the gate electrode layer of the transistor.

28. The device, as defined in claim 26, wherein the plurality of dummy gates layers are commonly connected on the substrate.

ABSTRACT

A layout method of a semiconductor device comprising the steps of: arranging active regions of a plurality of transistors having at least more than one first and second electrodes disposed on a substrate; arranging a plurality of gates of transistors between more than one first and second electrodes of those active regions respectively by positioning at least more than one gates having predetermined width and length at a constant gap on the substrate; and arranging a plurality of dummy gates having predetermined width and length between a plurality of transistors (or between and outside transistors) at the same gap as that of the gates of transistors on the substrate, so that all the gates of transistors are arranged at a constant gap to minimize the variances in process deviations and accordingly reduce the difference of threshold voltage of transistors, thereby increasing reliability of the semiconductor device.

FIG. 1(PRIOR ART)

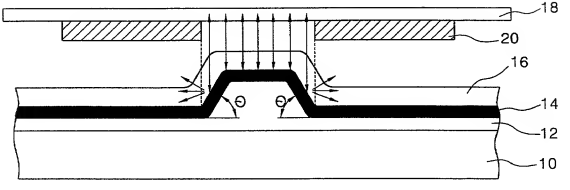


FIG. 2(PRIOR ART)

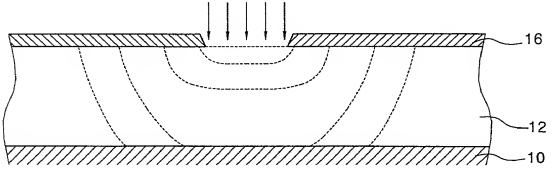


FIG. 3(PRIOR ART)

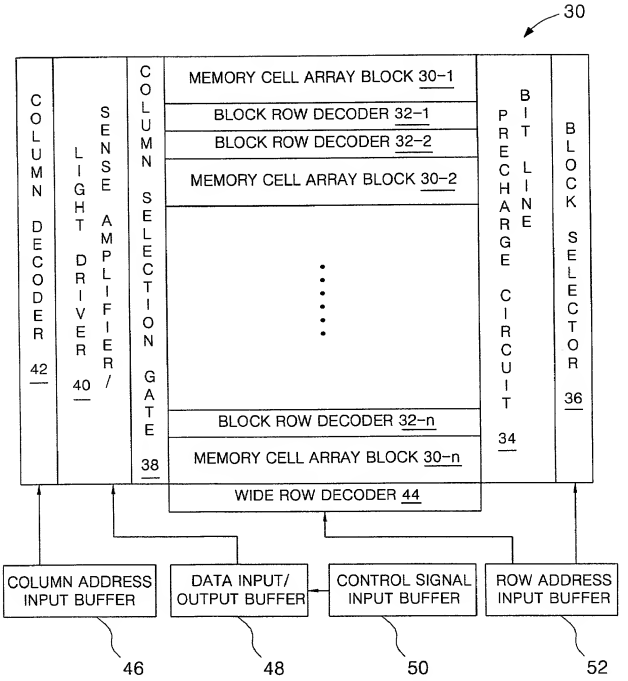


FIG. 4(PRIOR ART)

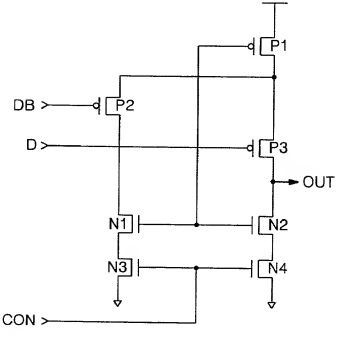


FIG. 5(PRIOR ART)

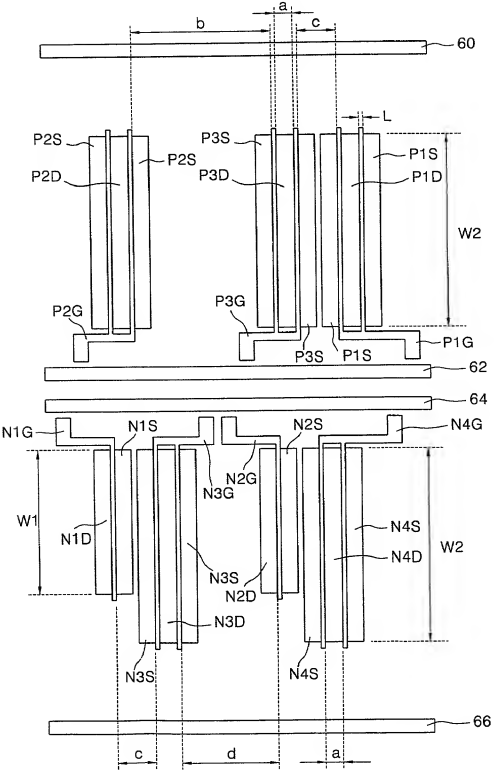


FIG. 6(PRIOR ART)

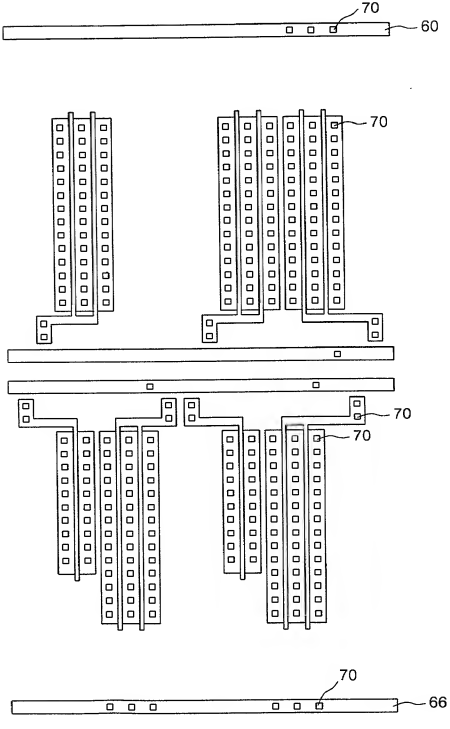


FIG. 7(PRIOR ART)

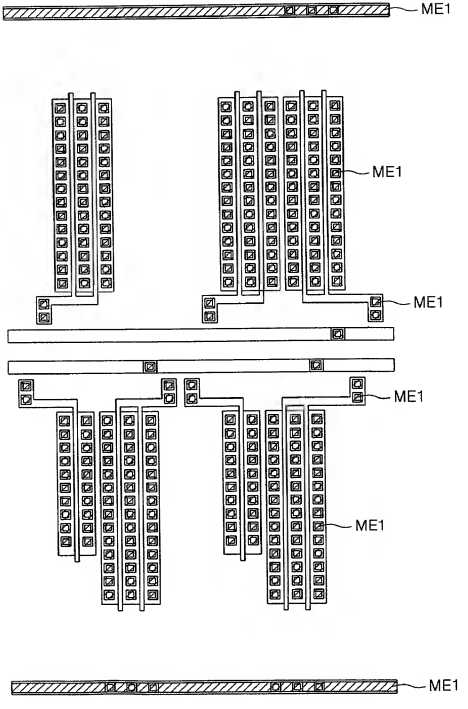


FIG. 8(PRIOR ART)

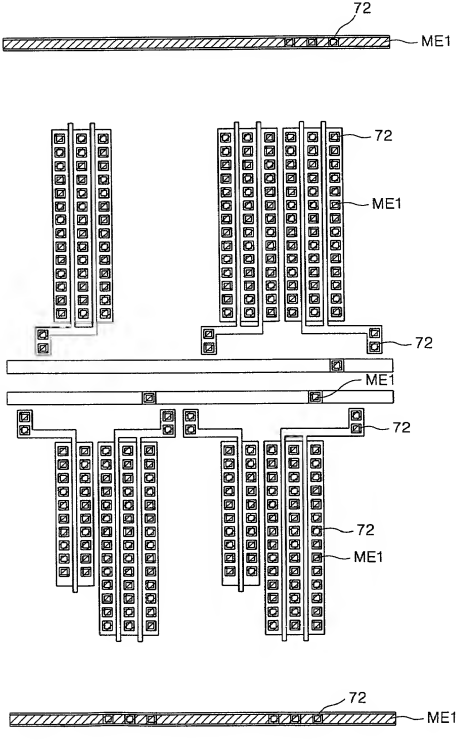


FIG. 9(PRIOR ART)

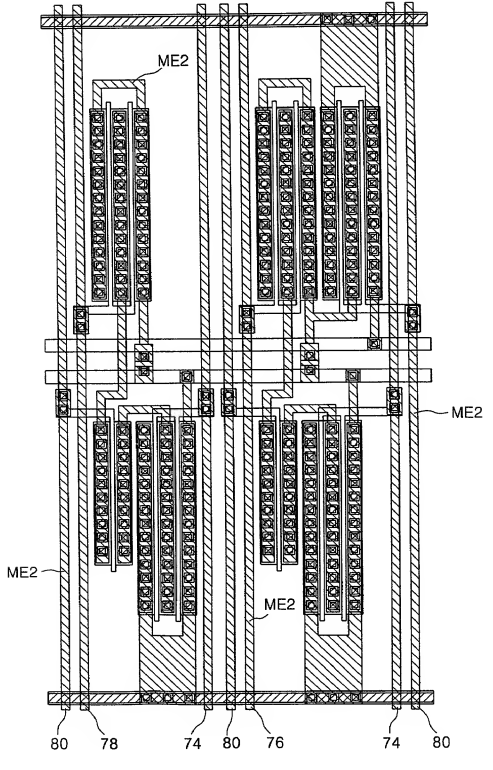


FIG. 10(PRIOR ART)

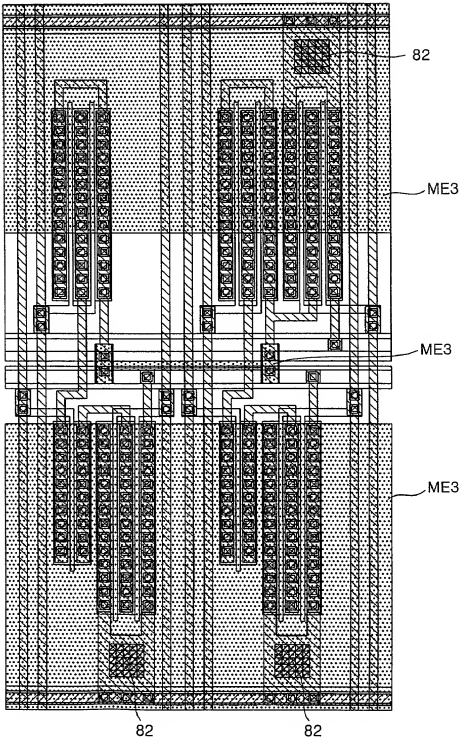


FIG. 11

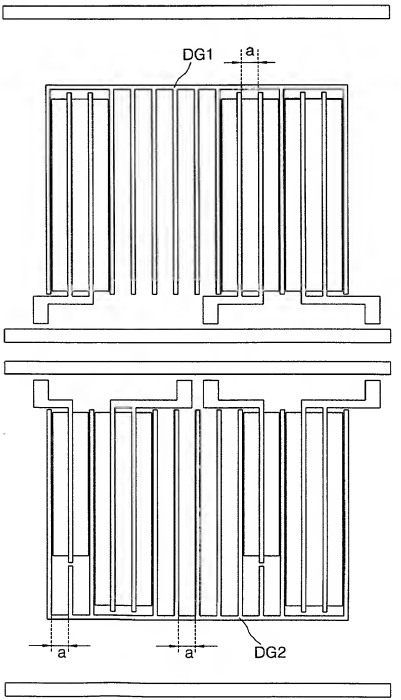
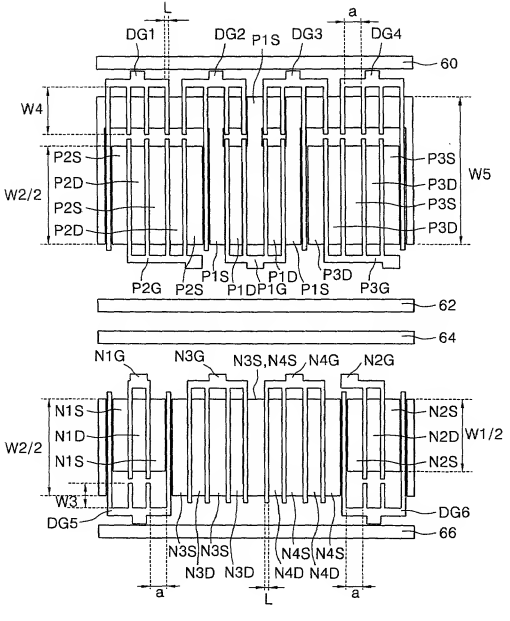


FIG. 12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DG2
P1S
DG3
DG4
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W4
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P2S
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P3D
P3S
P3D
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P2S
P1S
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P1G
P1S
P3D
P3G
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64
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N3G
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N4G
N2G
N1S
N1D
N1S
W2/2
N2S
N2D
N2S
W1/2
W3
DG5
DG6
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L
a

FIG. 13

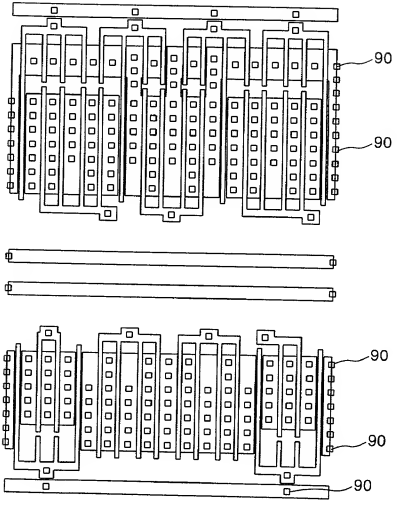


FIG. 14

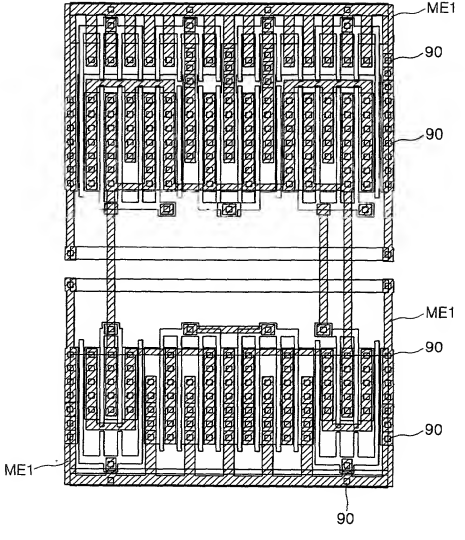


FIG. 15

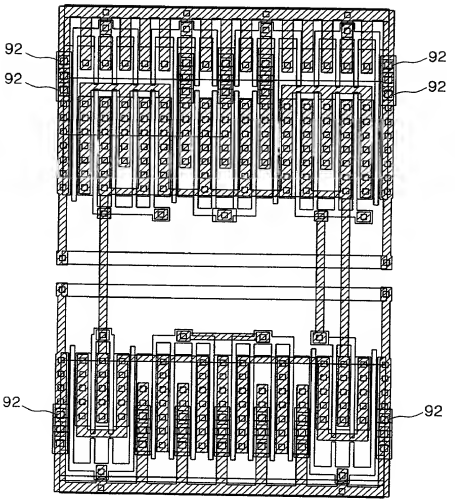


FIG. 16

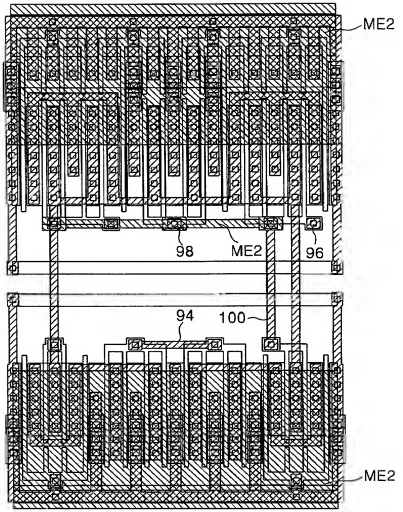


FIG. 17

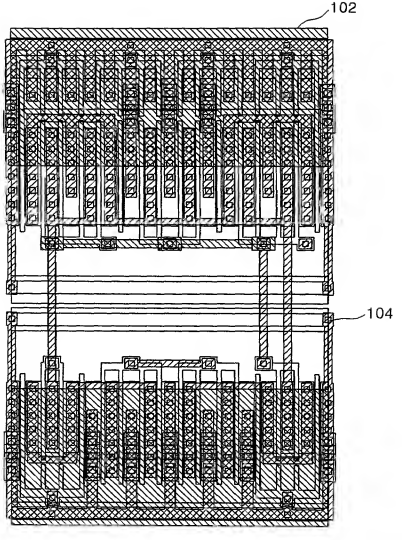
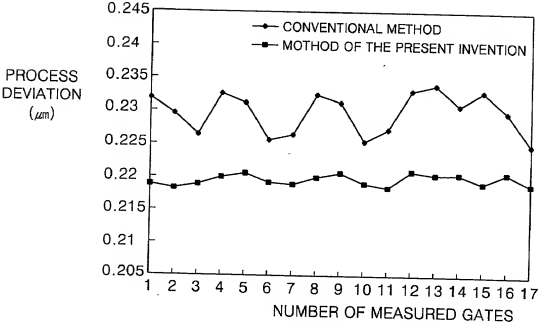


FIG. 18


CONVENTIONAL METHOD
MOTHOD OF THE PRESENT INVENTION
PROCESS DEVIATION (μm)
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0.24
0.235
0.23
0.225
0.22
0.215
0.21
0.205
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
NUMBER OF MEASURED GATES

PATENT APPLICATION
Attorney Docket No. 5484-53

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **LAYOUT METHOD OF SEMICONDUCTOR DEVICE**, the specification of which:

[X] is attached hereto.
[ ] was filed on _____ as Application No. _____
[ ] and was amended on _____(if applicable)
[ ] with amendments through _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 (a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Claiming Priority?
98-63134	Korea	31 December 1998	[X] Yes [ ] No
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under Title 35, United States Code, Sec. 119(e) of any United States provisional application listed below:

Provisional Application No.	Filing Date
_____	_____

I hereby claim the benefit under Title 35, United States Code, Sec. 120 or §365(c) of any PCT international application designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sec. 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute the application, to file a corresponding international application, to prosecute and transact all business in the Patent and Trademark Office connected therewith:

Customer No. 20575

Attorney Name	Registration No.
Jerome S. Marger	26,480
Alexander C. Johnson, Jr.	29,396
Alan T. McCollom	28,881
James G. Stewart	32,496
Glenn C. Brown	34,555
Stephen S. Ford	35,139
Gregory T. Kavounas	37,862
Scott A. Schaffer	38,610
Joseph S. Makuch	39,286
James E. Harris	40,013
Graciela G. Cowger	42,444
Ariel Rogson	43,054
Craig R. Rogers	43,888

Direct all telephone calls to Alan T. McCollom at (503) 222-3613 and send all correspondence to:

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, Oregon 97205

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: **Tae-Gyoung KANG**

Inventor's signature: Tae-Gyoung KANG

November 15, 1999
(Date)

Residence: Korea

Citizenship: Korea

Post Office address: #D-404, Daegwang villa, 1-19, Annyung-ri, Taian-eup, Whasung-kun, Kyungki-do, Rep. of Korea